LPDDR5X SDRAM

MT62F1G16D1, MT62F1G32D2, MT62F2G32D4, MT62F4G32D8, MT62F1G64D4, MT62F2G64D8

Features

- **Architecture**
  - 17.1 GB/s maximum bandwidth per channel
  - Frequency range: 1067–5 MHz (data rate range per pin: 8533–40 Mb/s with WCK:CK = 4:1)
  - Selectable CKR (WCK:CK = 2:1 or 4:1)
- **LPDDR5X/LPDDR5 data interface**
  - Single x16 channel/die
  - Double-data-rate command/address entry
  - Differential command clocks (CK_t/CK_c) for high-speed operation
  - Differential data clocks (WCK_t/WCK_c)
  - Optional differential read strobe (RDQS_t/RDQS_c)
  - 16*n*-bit or 32*n*-bit prefetch architecture
  - Bank Architecture: 8-bank (8B) mode, bank group (BG) mode, and 16-bank (16B) mode supported
  - Command-selectable burst lengths (BL = 16 or 32) in bank group or 16-bank modes
  - Background ZQ calibration/command-based ZQ calibration
  - Optional link protection (link ECC)
  - Partial-array self refresh (PASR) and partial-array auto refresh (PAAR) with segment mask
- **Ultra-low-voltage core and I/O power supplies**
  - V_{DD1} = 1.70–1.95V; 1.80V TYP
  - V_{DD2H} = 1.01–1.12V; 1.05V TYP
  - V_{DD2L} = V_{DD2H} or 0.87–0.97V; 0.90V TYP
  - V_{DDQ} = 0.50V or 0.45V[1] TYP; 0.30V TYP (ODT off only)
- **I/O characteristics**
  - Interface-LVSTL 0.5/0.3
  - I/O type: Low-swing single-ended, V_{SS} terminated
  - V_{OH}-compensated output drive
  - Programmable V_{SS} on-die termination (ODT)
  - Non target ODT support
  - DVFSQ support
- **Low power features**
  - DVFSC: Dynamic voltage frequency scaling core
  - Single-ended CK, single-ended WCK and single-ended RDQS
  - Data copy
  - Write X

Options	Marking
Operating Voltage	F
– V_{DD1}/V_{DD2H}/V_{DD2L}/V_{DDQ}/V_{DDQ} (ODT off only): 1.80V/1.05V/V_{DD2H} or 0.90V/0.50V or 0.45V[1]/0.30V	
Array Configuration	
– 1 Gig x 16 (1Gx16 x 1 Ch x 1R)	1G16
– 1 Gig x 32 (1Gx16 x 2 Ch x 1R)	1G32
– 2 Gig x 32 (1Gx16 x 2 Ch x 2R)	2G32
– 4 Gig x 32 (2Gx8 x 2 Ch x 2R)	4G32
– 1Gig x 64 (1Gx16 x 4 Ch x 1R)	1G64
– 2 Gig x 64 (1Gx16 x 4 Ch x 2R)	2G64
Device configuration	
– 1 die in package (1G16 x 1 die)	D1
– 2 die in package (1G16 x 2 die)	D2
– 4 die in package (1G16 x 4 die)	D4
– 8 die in package (2G8 x 8 die)	D8
– 8 die in package (1G16 x 8 die)	D8
FBGA RoHS-compliant "green" package	
– 315-ball TFBGA 12.4mm x 15.0mm (TYP), seated height 1.1mm (MAX)	DS
– 315-ball LFBGA 12.4mm x 15.0mm (TYP), seated height 1.3mm (MAX)	DV
– 441-ball TFBGA 14.0mm x 14.0mm (TYP), seated height 1.1mm (MAX)	EK
Speed grade, cycle time (^{t}WCK)	
– 8533 Mb/s	-023
– 7500 Mb/s	-026
Operating Temperature:	
– –25°C ≤ T_C ≤ +85°C	WT
– –40°C ≤ T_C ≤ +95°C	IT
Revision	:B

Note: 1. V_{DDQ} = 0.45V (TYP) only supported in 441-ball package up to 6400 Mb/s.

Part Number Ordering Information

Figure 1: Part Number Chart

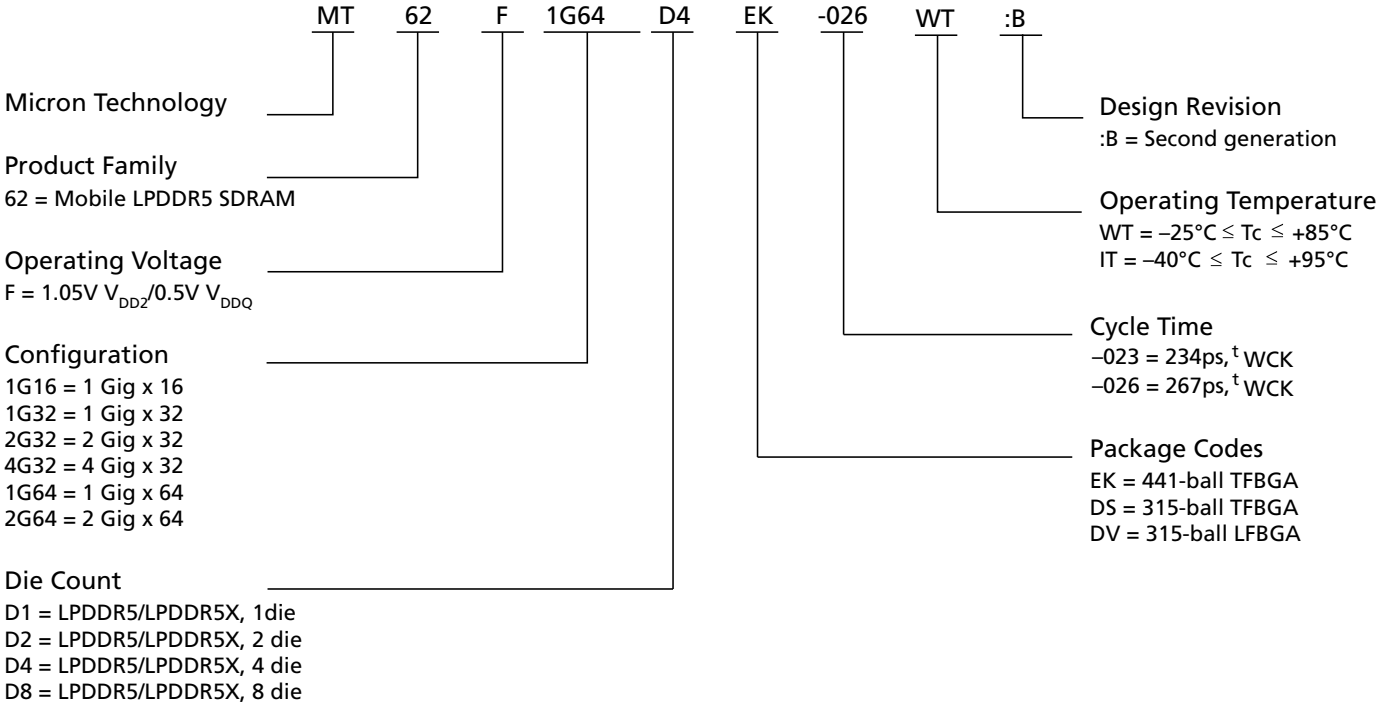

Table 1: Part Number List

Part Number	Total Density	Data Rate per Pin
MT62F1G16D1DS-023 IT:B	2GB (16Gb)	8533 Mb/s
MT62F1G32D2DS-023 IT:B	4GB (32Gb)	
MT62F1G32D2DS-023 WT:B		
MT62F2G32D4DS-023 IT:B	8GB (64Gb)	
MT62F2G32D4DS-023 WT:B		
MT62F4G32D8DV-023 IT:B	16GB (128Gb)	
MT62F4G32D8DV-023 WT:B		
MT62F1G64D4EK-023 WT:B	8GB (64Gb)	
MT62F2G64D8EK-023 WT:B	16GB (128Gb)	
MT62F1G32D2DS-026 WT:B	4GB (32Gb)	7500 Mb/s
MT62F2G32D4DS-026 WT:B	8GB (64Gb)	
MT62F4G32D8DV-026 WT:B	16GB (128Gb)	
MT62F1G64D4EK-026 WT:B	8GB (64Gb)	
MT62F2G64D8EK-026 WT:B	16GB (128Gb)	

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.

LPDDR5/LPDDR5X Data Sheet List

For general LPDDR5/LPDDR5X specifications, please refer to the data sheets below.

- General LPDDR5/LPDDR5X Specifications 1: Mode Registers
- General LPDDR5/LPDDR5X Specifications 2: AC/DC and Interface Specifications
- General LPDDR5/LPDDR5X Specifications 3: Features and Functionalities

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General Notes

Throughout the data sheet, figures and text refer to DQs as DQ. DQ should be interpreted as any or all DQs collectively, unless specifically stated otherwise.

RDQS, CK, and WCK should be interpreted as RDQS_t, RDQS_c, CK_t, CK_c, and WCK_t, WCK_c respectively unless specifically stated otherwise. CA includes all CA pins used for a given density.

In timing diagrams, CMD is used as an indicator only. Actual signals occur on CA[6:0].

V_{REF} indicates $V_{REF(CA)}$ and $V_{REF(DQ)}$.

Complete functionality is described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.

Device Configuration

Table 2: Die Organization in the Package (x16)

Die Organization	1G16 (16 Gb/package)
Channel A	x16 mode × 1 die

Note: 1. Refer to the Package Block Diagram section in this data sheet.

Table 3: Die Organization in the Package (x32)

Die Organization	1G32 (32 Gb/package)	2G32 (64 Gb/package)	4G32 (128 Gb/package)
Channel A	x16 mode × 1 die	–	–
Channel B	x16 mode × 1 die	–	–
Channel A, rank 0	–	x16 mode × 1 die	–
Channel B, rank 0	–	x16 mode × 1 die	–
Channel A, rank 1	–	x16 mode × 1 die	–
Channel B, rank 1	–	x16 mode × 1 die	–
Channel A, rank 0 DQ[7:0]	–	–	x8 mode × 1 die
Channel A, rank 1 DQ[7:0]	–	–	x8 mode × 1 die
Channel B, rank 0 DQ[7:0]	–	–	x8 mode × 1 die
Channel B, rank 1 DQ[7:0]	–	–	x8 mode × 1 die
Channel A, rank 0 DQ[15:8]	–	–	x8 mode × 1 die
Channel A, rank 1 DQ[15:8]	–	–	x8 mode × 1 die
Channel B, rank 0 DQ[15:8]	–	–	x8 mode × 1 die
Channel B, rank 1 DQ[15:8]	–	–	x8 mode × 1 die

Note: 1. Refer to the Package Block Diagram section in this data sheet.

Table 4: Die Organization in the Package (x64)

Die Organization	1G64 (64 Gb/package)	2G64 (128 Gb/package)
Channel A, rank 0	x16 mode × 1 die	x16 mode × 1 die
Channel B, rank 0	x16 mode × 1 die	x16 mode × 1 die
Channel C, rank 0	x16 mode × 1 die	x16 mode × 1 die
Channel D, rank 0	x16 mode × 1 die	x16 mode × 1 die
Channel A, rank 1	–	x16 mode × 1 die
Channel B, rank 1	–	x16 mode × 1 die
Channel C, rank 1	–	x16 mode × 1 die
Channel D, rank 1	–	x16 mode × 1 die

Note: 1. Refer to the Package Block Diagram section in this data sheet.

Table 5: Die Addressing

Description	1G16 (16Gb/package), 1G32 (32 Gb/package), 2G32 (64 Gb/package), 1G64 (64 Gb/package), 2G64 (128 Gb/package)			4G32 (128Gb/package)		
Density per die	16Gb			16Gb		
Bits	17,179,869,184			17,179,869,184		
Bank mode	BG mode	16B mode	8B mode	BG mode	16B mode	8B mode
Configuration	64Mb × 16 DQ × 4 Banks × 4BG	64Mb × 16 DQ × 16 Banks	128Mb × 16 DQ × 8 Banks	128Mb × 8 DQ × 4 Banks × 4BG	128Mb × 8 DQ × 16 Banks	256Mb × 8 DQ × 8 Banks
Number of banks	4	16	8	4	16	8
Number of bank groups	4	1	1	4	1	1
Array prefetch bits	256	256	512	128	128	256
Rows per bank	65,536			131,072		
Columns	64			64		
Page size (bytes)	2048	2048	4096	1024	1024	2048
Native burst length	16	16	32	16	16	32
Number of I/Os	16			8		
Bank address	BA[1:0]	BA[3:0]	BA[2:0]	BA[1:0]	BA[3:0]	BA[2:0]
Bank group address	BG[1:0]	–	–	BG[1:0]	–	–
Row address	R[15:0]			R[16:0]		
Column address	C[5:0]			C[5:0]		
Burst address	B[3:0]	B[3:0]	B[4:0]	B[3:0]	B[3:0]	B[4:0]
Burst starting address boundary	128-bit			128-bit		

Note: 1. Refer to the SDRAM Addressing section in General LPDDR5/LPDDR5X Specifications 3.

Refresh Requirement Parameters

Table 6: Refresh Requirement Parameters

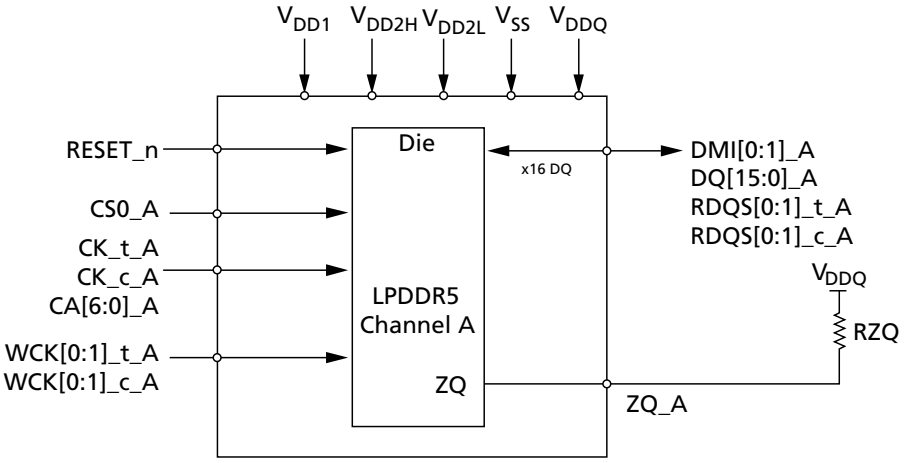
Parameter	Symbol	16Gb Die		Unit
		BG and 16B Mode	8B Mode	
REFRESH cycle time (all banks)	^{t}RFCab	280	280	ns
REFRESH cycle time (per bank)	^{t}RFCpb	140	140	ns
Per bank refresh to per bank refresh time (different bank)	^{t}PBR2PBR	90	90	ns
Per bank refresh to ACTIVATE command time (different bank)	^{t}PBR2ACT	7.5	10	ns

Note: 1. This table only describes refresh parameters that are density dependent. Refer to Refresh Requirement section in General LPDDR5/LPDDR5X Specifications 3 for all refresh parameters.

Package Block Diagrams

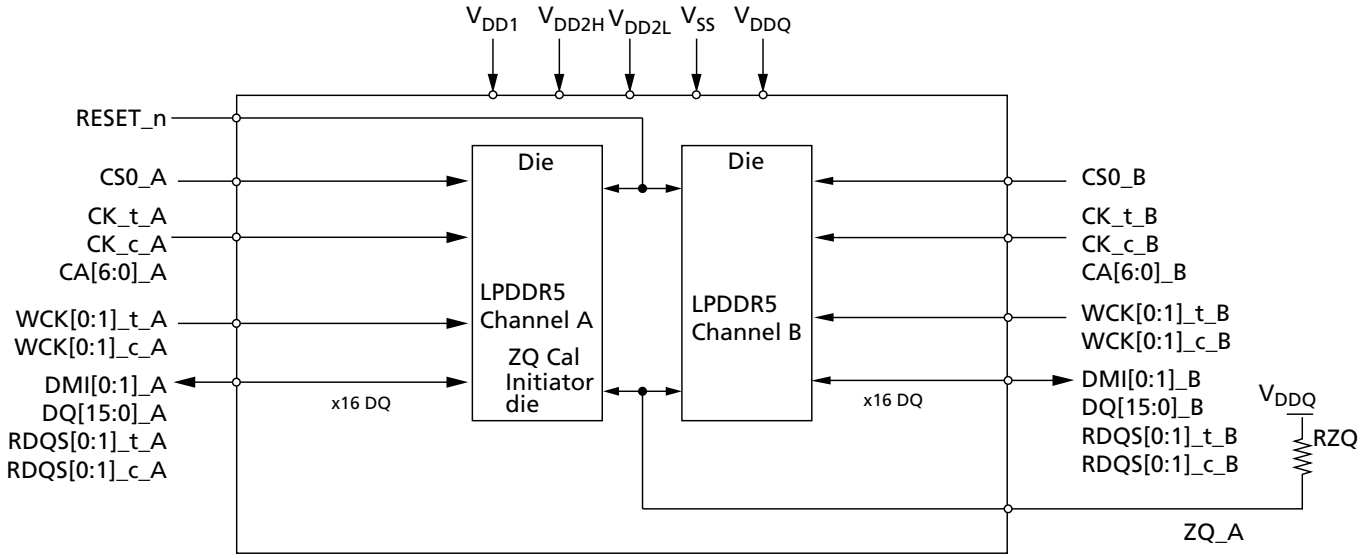
Single Die, Single Channel, Single Rank

Figure 2: Single-Die, Single-Channel, Single-Rank Package Block Diagram



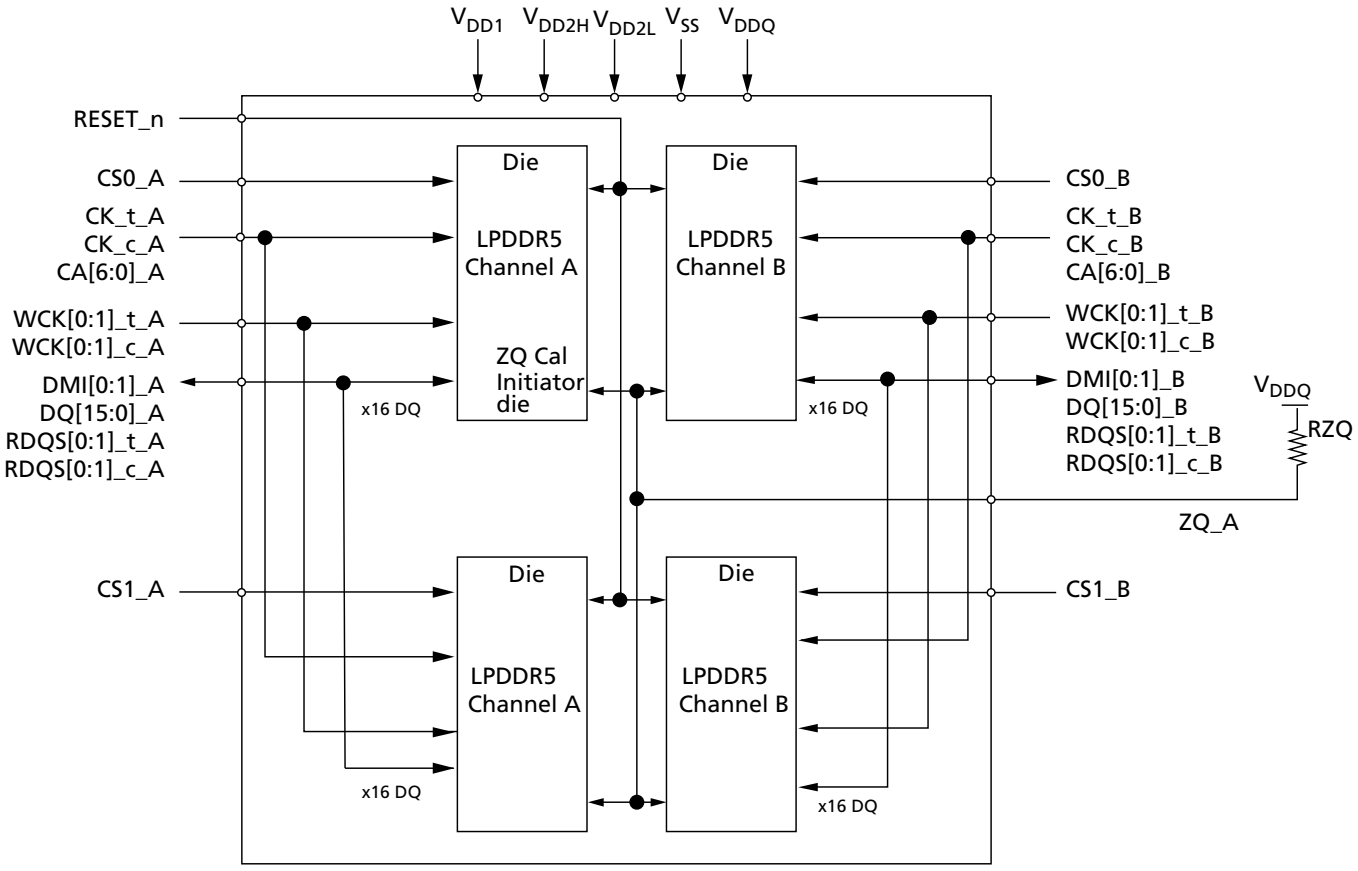
Dual Die, Dual Channel, Single Rank

Figure 3: Dual-Die, Dual-Channel, Single-Rank Package Block Diagram



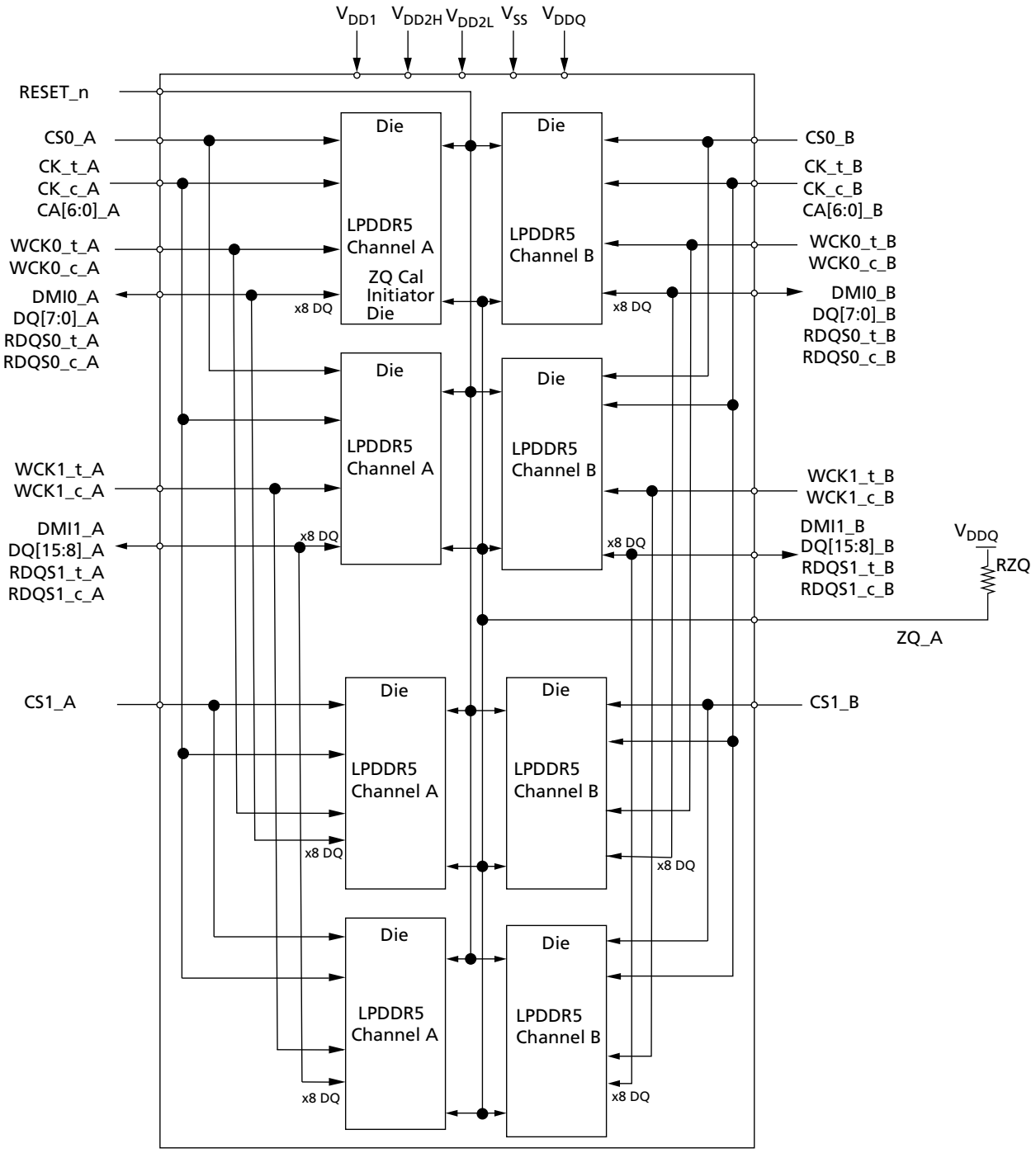
Quad Die, Dual Channel, Dual Rank

Figure 4: Quad-Die, Dual-Channel, Dual-Rank Package Block Diagram



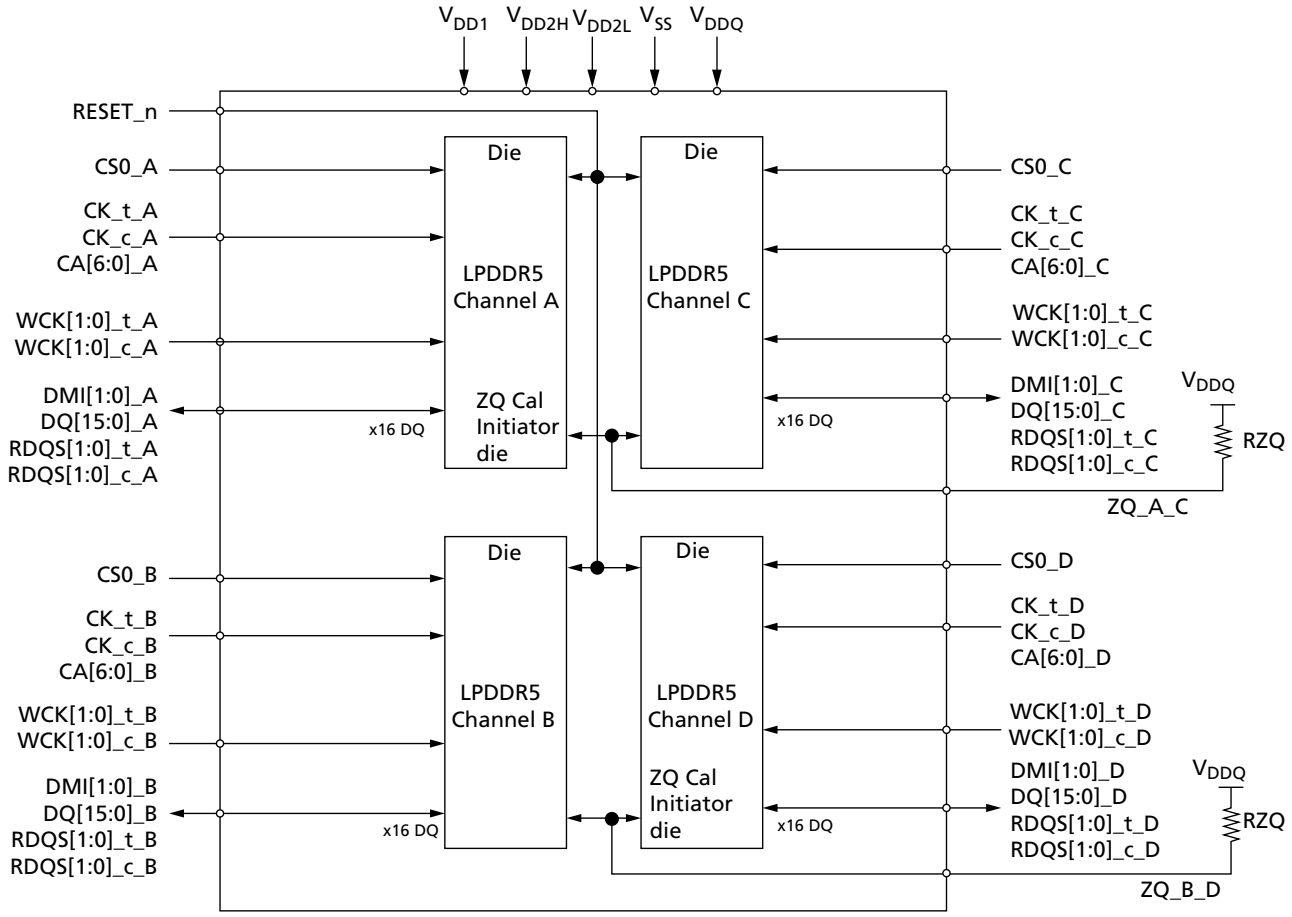
Eight Die, Dual Channel, Dual Rank

Figure 5: Eight-Die, Dual-Channel, Dual-Rank Package Block Diagram



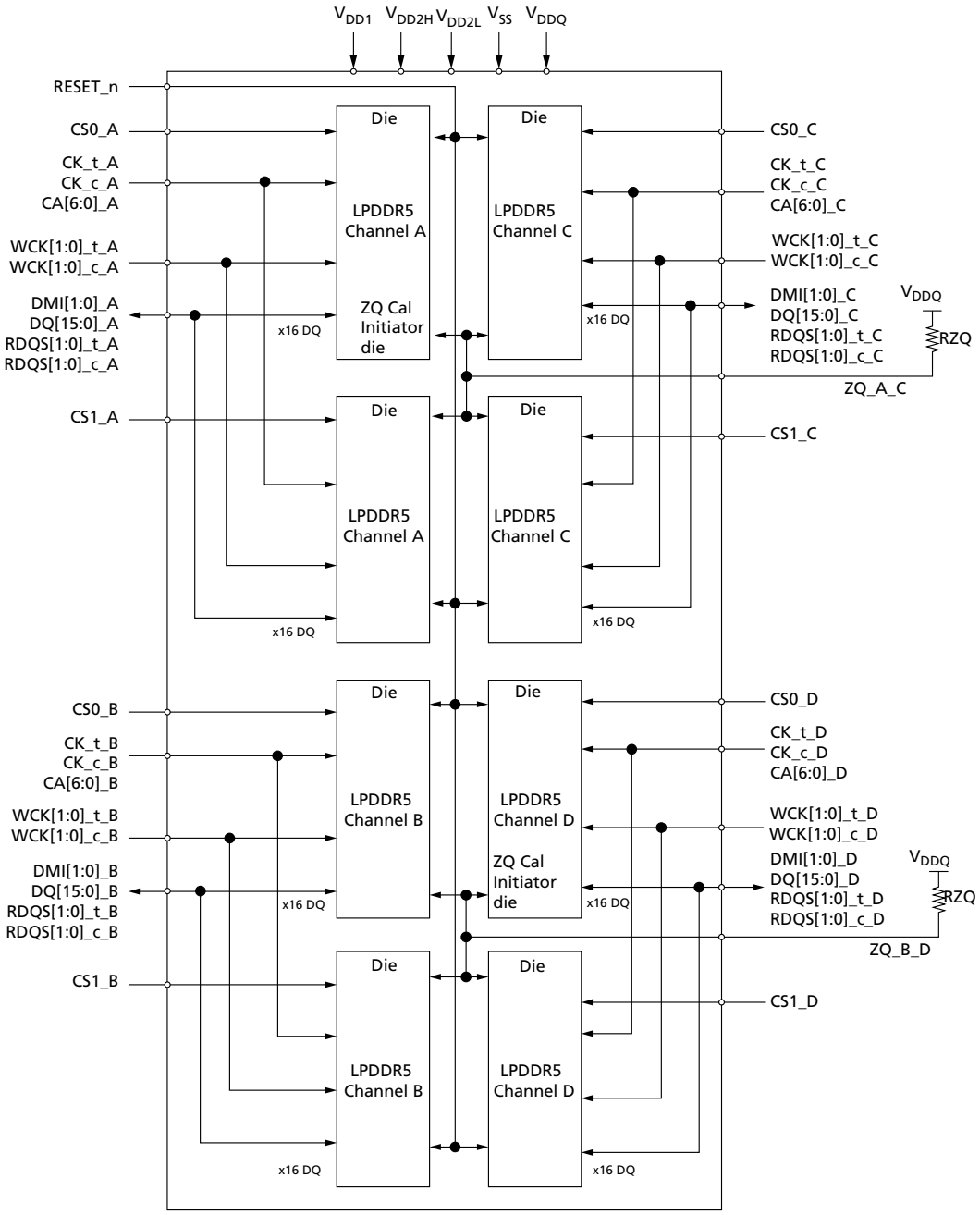
Quad Die, Quad Channel, Single Rank

Figure 6: Quad-Die, Quad-Channel, Single-Rank Package Block Diagram



Eight Die, Quad Channel, Dual Rank

Figure 7: Eight-Die, Quad-Channel, Dual-Rank Package Block Diagram



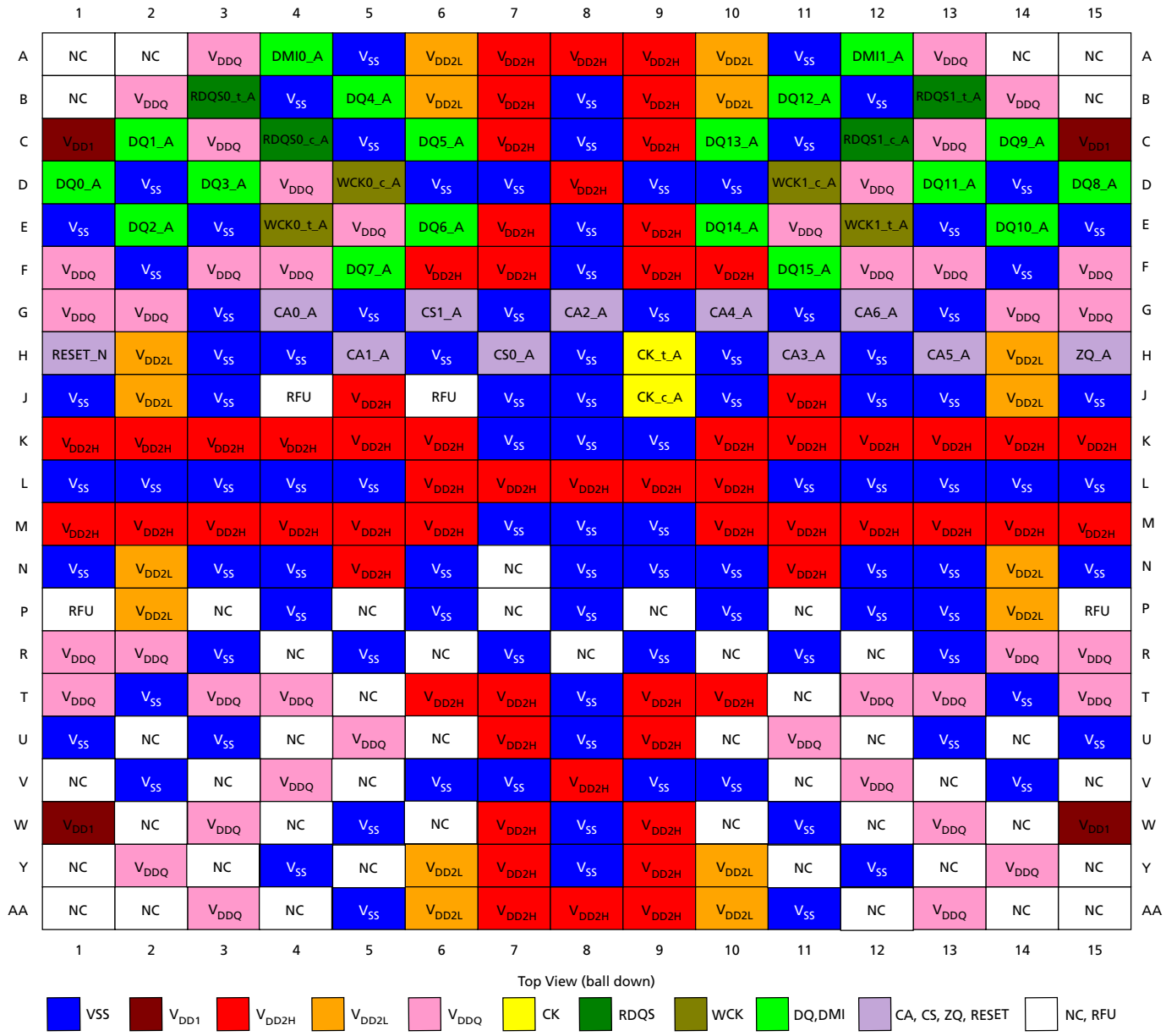
Ball Assignments and Descriptions

315b Single Die, Single Channel, 1 Rank

Table 7: Single Channel 315-Ball/Pad Descriptions

Symbol	Type	Description
CK_t_[A], CK_c_[A]	Input	**Clock:** CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS0_[A], CS1_[A]	Input	**Chip select:** CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:B] become NC pins in a single-rank package.
CA[6:0]_[A]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
WCK[1:0]_t_[A], WCK[1:0]_c_[A]	Input	**Data clock:** WCK_t and WCK_c are differential clock inputs used for write data capture and read data output.
DQ[15:0]_[A]	I/O	**Data input/output:** Bidirectional data bus.
RDQS[1:0]_t_[A], RDQS[1:0]_c_[A]	I/O Output	**Read data strobe:** RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals.
DMI[1:0]_[A]	I/O	**Data mask inversion:** DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
ZQ_A	Reference	**ZQ calibration reference:** Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to V_{DDQ} through a 240Ω ±1% resistor.
V_{DDQ}, V_{DD1}, V_{DD2H}, V_{DD2L}	Supply	**Power supplies:** Isolated on the die for improved noise immunity.
V_{SS}	Supply	**Ground reference:** Power supply ground reference.
RESET_n	Input	**Reset:** When asserted LOW, the RESET pin resets the die. Reset is an asynchronous signal.
NC	–	**No connect:** Not internally connected.
RFU	–	**Reserved Future Use:** Not internally connected

Figure 8: 315-Ball Single-Channel Discrete FBGA



315b Dual Channel, 1 Rank, 2 Rank

Table 8: 315-Ball/Pad Descriptions

Symbol	Type	Description
CK_t_[A:B], CK_c_[A:B]	Input	**Clock:** CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS0_[A:B], CS1_[A:B]	Input	**Chip select:** CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:B] become NC pins in a single-rank package.
CA[6:0]_[A:B]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
WCK[1:0]_t_[A:B], WCK[1:0]_c_[A:B]	Input	**Data clock:** WCK_t and WCK_c are differential clock inputs used for write data capture and read data output.
DQ[15:0]_[A:B]	I/O	**Data input/output:** Bidirectional data bus.
RDQS[1:0]_t_[A:B], RDQS[1:0]_c_[A:B]	I/O Output	**Read data strobe:** RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals.
DMI[1:0]_[A:B]	I/O	**Data mask inversion:** DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
ZQ_A	Reference	**ZQ calibration reference:** Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to V_{DDQ} through a 240Ω ±1% resistor.
V_{DDQ}, V_{DD1}, V_{DD2H}, V_{DD2L}	Supply	**Power supplies:** Isolated on the die for improved noise immunity.
V_{SS}	Supply	**Ground reference:** Power supply ground reference.
RESET_n	Input	**Reset:** When asserted LOW, the RESET pin resets the die. Reset is an asynchronous signal.
NC	–	**No connect:** Not internally connected.
RFU	–	**Reserved Future Use:** Not internally connected.

Figure 9: 315-Ball Dual-Channel Discrete FBGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	NC	NC	V_{DDQ}	DMI0_A	V_{SS}	V_{DD2L}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2L}	V_{SS}	DMI1_A	V_{DDQ}	NC	NC	A
B	NC	V_{DDQ}	RDQS0_t_A	V_{SS}	DQ4_A	V_{DD2L}	V_{DD2H}	V_{SS}	V_{DD2H}	V_{DD2L}	DQ12_A	V_{SS}	RDQS1_t_A	V_{DDQ}	NC	B
C	V_{DD1}	DQ1_A	V_{DDQ}	RDQS0_c_A	V_{SS}	DQ5_A	V_{DD2H}	V_{SS}	V_{DD2H}	DQ13_A	V_{SS}	RDQS1_c_A	V_{DDQ}	DQ9_A	V_{DD1}	C
D	DQ0_A	V_{SS}	DQ3_A	V_{DDQ}	WCK0_c_A	V_{SS}	V_{SS}	V_{DD2H}	V_{SS}	V_{SS}	WCK1_c_A	V_{DDQ}	DQ11_A	V_{SS}	DQ8_A	D
E	V_{SS}	DQ2_A	V_{SS}	WCK0_t_A	V_{DDQ}	DQ6_A	V_{DD2H}	V_{SS}	V_{DD2H}	DQ14_A	V_{DDQ}	WCK1_t_A	V_{SS}	DQ10_A	V_{SS}	E
F	V_{DDQ}	V_{SS}	V_{DDQ}	V_{DDQ}	DQ7_A	V_{DD2H}	V_{DD2H}	V_{SS}	V_{DD2H}	V_{DD2H}	DQ15_A	V_{DDQ}	V_{DDQ}	V_{SS}	V_{DDQ}	F
G	V_{DDQ}	V_{DDQ}	V_{SS}	CA0_A	V_{SS}	CS1_A	V_{SS}	CA2_A	V_{SS}	CA4_A	V_{SS}	CA6_A	V_{SS}	V_{DDQ}	V_{DDQ}	G
H	RESET_N	V_{DD2L}	V_{SS}	V_{SS}	CA1_A	V_{SS}	CS0_A	V_{SS}	CK_t_A	V_{SS}	CA3_A	V_{SS}	CA5_A	V_{DD2L}	ZQ_A	H
J	V_{SS}	V_{DD2L}	V_{SS}	RFU	V_{DD2H}	RFU	V_{SS}	V_{SS}	CK_c_A	V_{SS}	V_{DD2H}	V_{SS}	V_{SS}	V_{DD2L}	V_{SS}	J
K	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{SS}	V_{SS}	V_{SS}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	K
L	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	L
M	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{SS}	V_{SS}	V_{SS}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	M
N	V_{SS}	V_{DD2L}	V_{SS}	V_{SS}	V_{DD2H}	V_{SS}	CK_c_B	V_{SS}	V_{SS}	V_{SS}	V_{DD2H}	V_{SS}	V_{SS}	V_{DD2L}	V_{SS}	N
P	RFU	V_{DD2L}	CA5_B	V_{SS}	CA3_B	V_{SS}	CK_t_B	V_{SS}	CS0_B	V_{SS}	CA1_B	V_{SS}	V_{SS}	V_{DD2L}	RFU	P
R	V_{DDQ}	V_{DDQ}	V_{SS}	CA6_B	V_{SS}	CA4_B	V_{SS}	CA2_B	V_{SS}	CS1_B	V_{SS}	CA0_B	V_{SS}	V_{DDQ}	V_{DDQ}	R
T	V_{DDQ}	V_{SS}	V_{DDQ}	V_{DDQ}	DQ15_B	V_{DD2H}	V_{DD2H}	V_{SS}	V_{DD2H}	V_{DD2H}	DQ7_B	V_{DDQ}	V_{DDQ}	V_{SS}	V_{DDQ}	T
U	V_{SS}	DQ10_B	V_{SS}	WCK1_t_B	V_{DDQ}	DQ14_B	V_{DD2H}	V_{SS}	V_{DD2H}	DQ6_B	V_{DDQ}	WCK0_t_B	V_{SS}	DQ2_B	V_{SS}	U
V	DQ8_B	V_{SS}	DQ11_B	V_{DDQ}	WCK1_c_B	V_{SS}	V_{SS}	V_{DD2H}	V_{SS}	V_{SS}	WCK0_c_B	V_{DDQ}	DQ3_B	V_{SS}	DQ0_B	V
W	V_{DD1}	DQ9_B	V_{DDQ}	RDQS1_c_B	V_{SS}	DQ13_B	V_{DD2H}	V_{SS}	V_{DD2H}	DQ5_B	V_{SS}	RDQS0_c_B	V_{DDQ}	DQ1_B	V_{DD1}	W
Y	NC	V_{DDQ}	RDQS1_t_B	V_{SS}	DQ12_B	V_{DD2L}	V_{DD2H}	V_{SS}	V_{DD2H}	V_{DD2L}	DQ4_B	V_{SS}	RDQS0_t_B	V_{DDQ}	NC	Y
AA	NC	NC	V_{DDQ}	DMI1_B	V_{SS}	V_{DD2L}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2L}	V_{SS}	DMI0_B	V_{DDQ}	NC	NC	AA
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Top View (ball down)

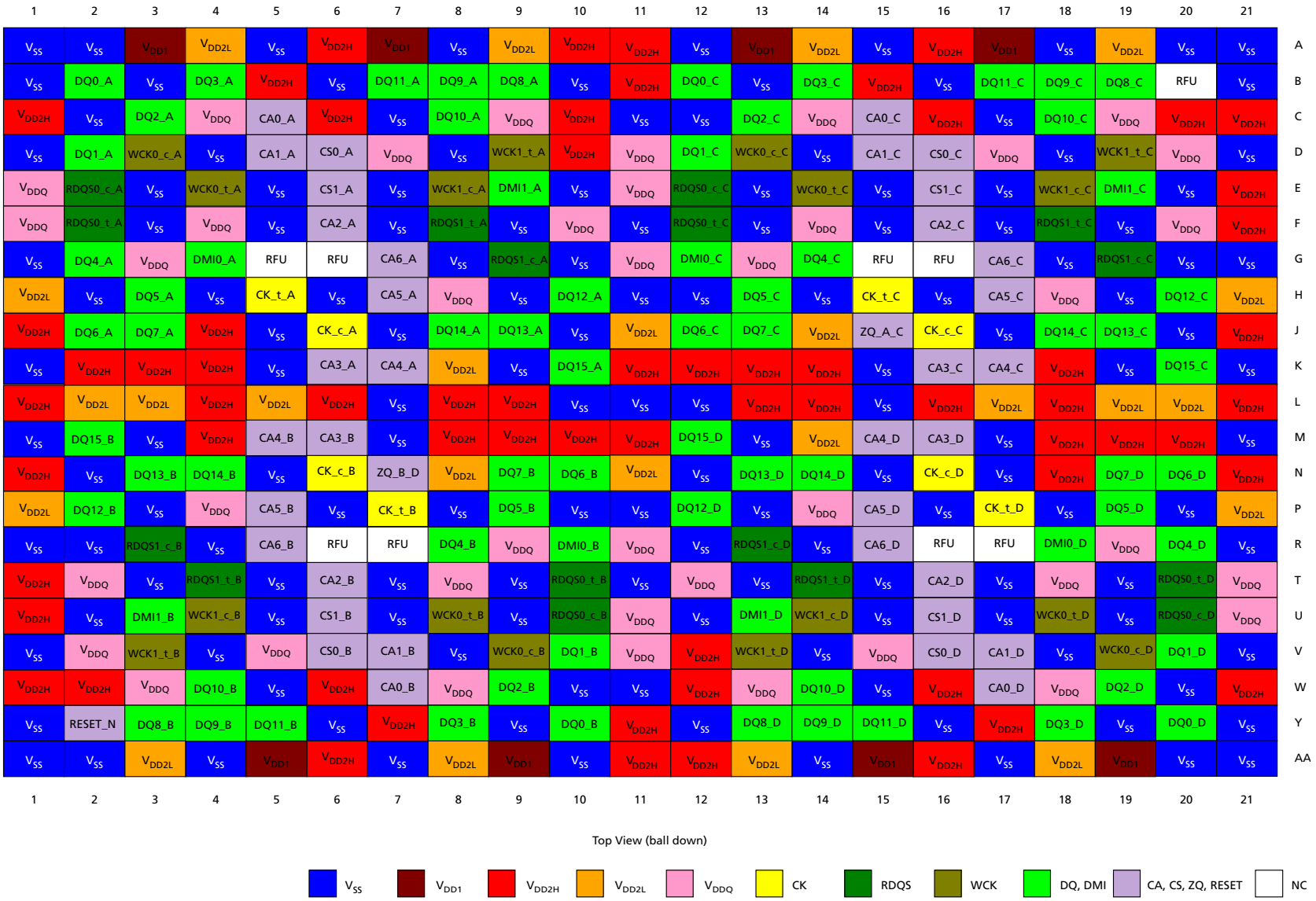
VSS | V_{DD1} | V_{DD2H} | V_{DD2L} | V_{DDQ} | CK | RDQS | WCK | DQ,DMI | CA, CS, ZQ, RESET | NC, RFU

441b Quad Channel, 1 Rank, 2 Rank

Table 9: 441-Ball/Pad Descriptions

Symbol	Type	Description
CK_t_[A:D], CK_c_[A:D]	Input	**Clock:** CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS0_[A:D], CS1_[A:D]	Input	**Chip select:** CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:D] become NC pins in a single-rank package.
CA[6:0]_[A:D]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
WCK[1:0]_t_[A:D], WCK[1:0]_c_[A:D]	Input	**Data clock:** WCK_t and WCK_c are differential clock inputs used for WRITE data capture and READ data output.
DQ[15:0]_[A:D]	I/O	**Data input/output:** Bidirectional data bus.
RDQS[1:0]_t_[A:D], RDQS[1:0]_c_[A:D]	I/O Output	**Read data strobe:** RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals.
DMI[1:0]_[A:D]	I/O	**Data mask inversion:** DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
ZQ_A_C, ZQ_B_D	Reference	**ZQ calibration reference:** Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to V_{DDQ} through a 240Ω ±1% resistor.
V_{DDQ}, V_{DD1}, V_{DD2H}, V_{DD2L}	Supply	**Power supplies:** Isolated on the die for improved noise immunity.
V_{SS}	Supply	**Ground reference:** Power supply ground reference.
RESET_n	Input	**Reset:** When asserted LOW, the RESET pin resets the die. Reset is an asynchronous signal.
NC	–	**No connect:** Not internally connected.
RFU	–	**Reserved Future Use:** Not internally connected

Figure 10: 441-Ball Quad-Channel FBGA



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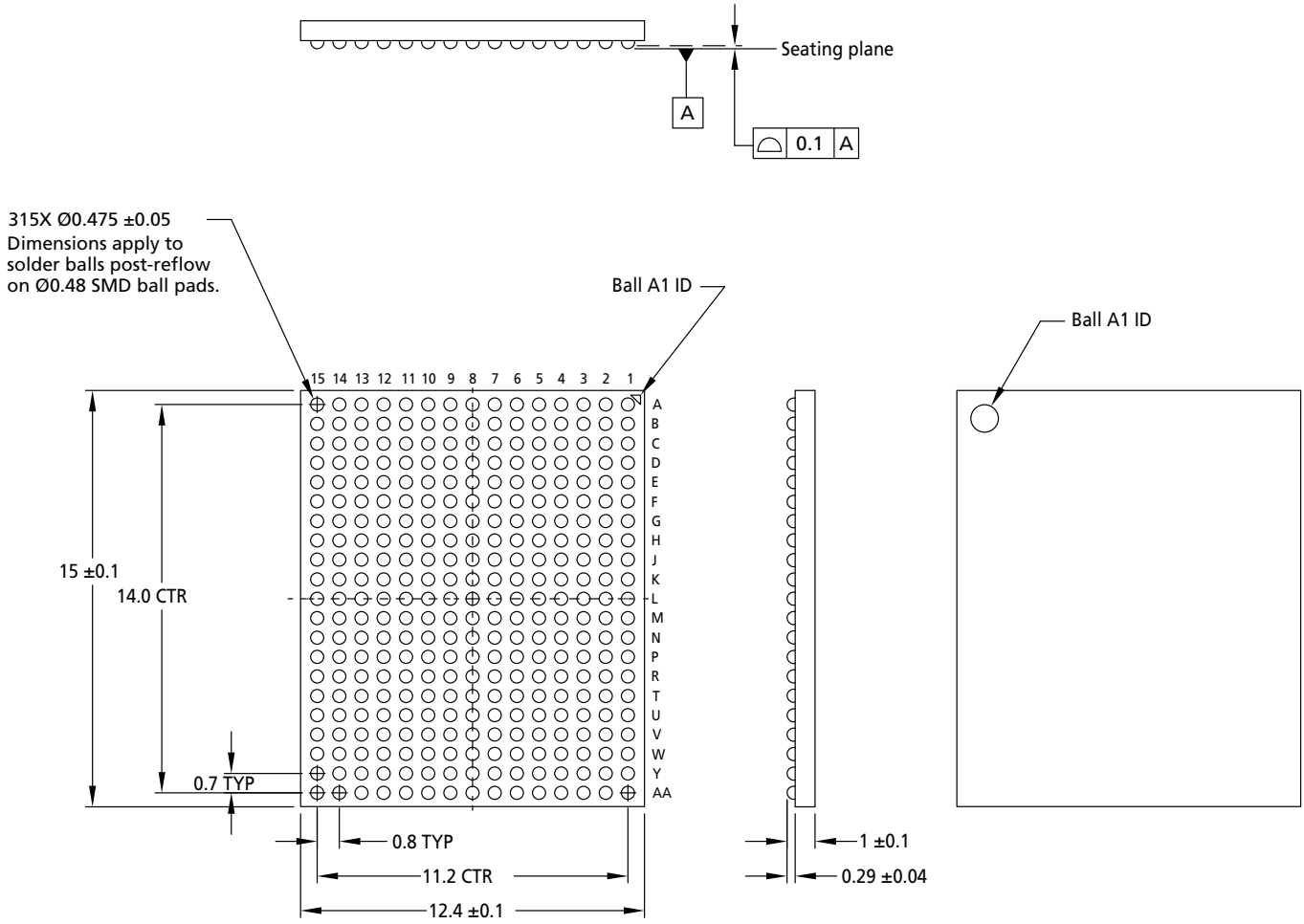
315b_441b_y42m_sdp_ddp_qdp_8dp_lpddr5x_it_wt.pdf - Rev. D 11/2022 EN

Package Dimensions

315-Ball Package (Package Code: DS)

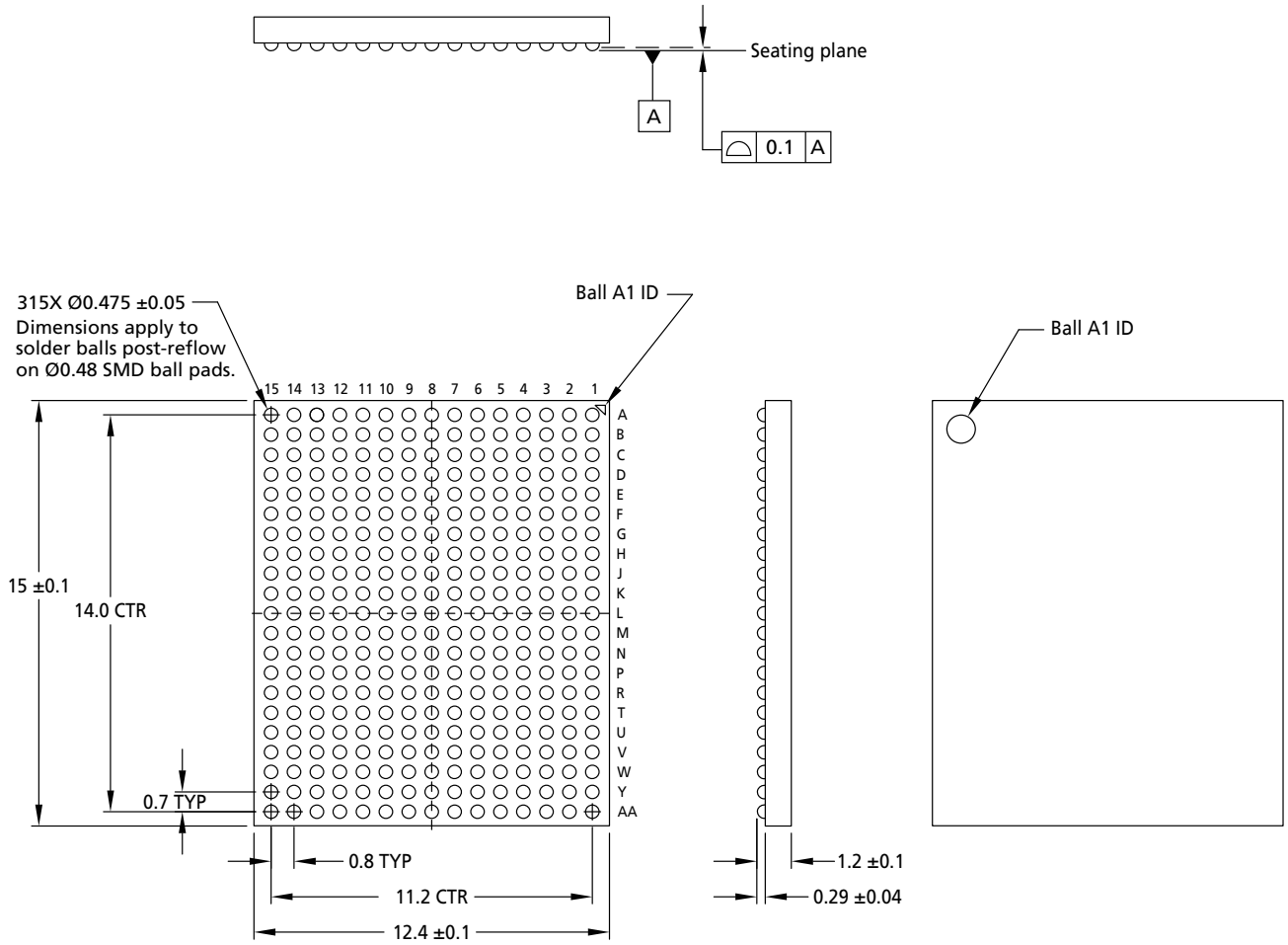
Figure 11: 315-Ball TFBGA – 12.4mm (TYP) × 15.0mm (TYP) × 1.1mm (MAX) (Package Code: DS)



Notes: 1. All dimensions are in millimeters.
2. Solder ball composition: SACQ with CuOSP pads (Sn-4Ag-0.5Cu-3Bi-0.05Ni)

315-Ball Package (Package Code: DV)

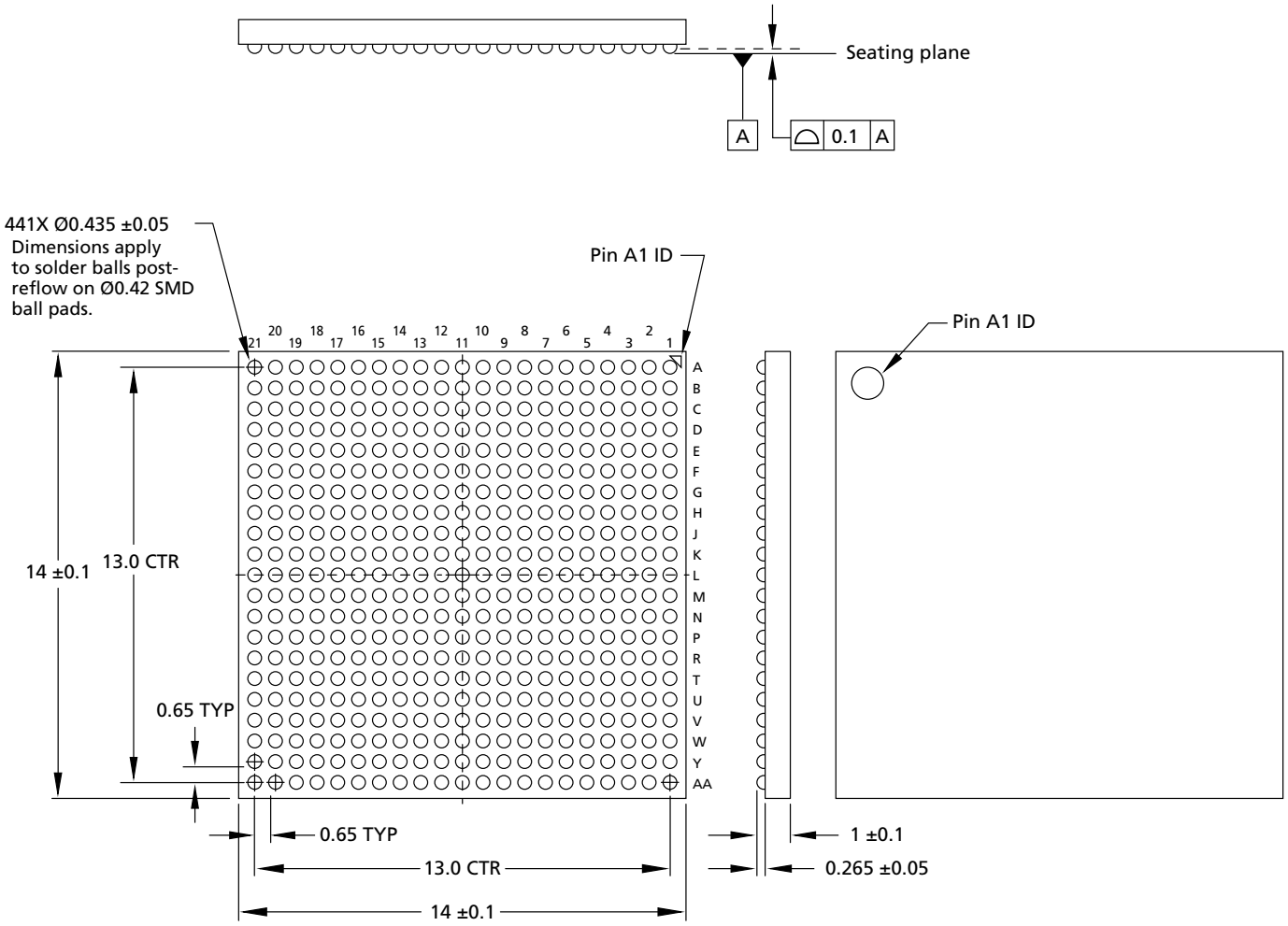
Figure 12: 315-Ball LFBGA – 12.4mm (TYP) × 15.0mm (TYP) × 1.3mm (MAX) (Package Code: DV)



Notes: 1. All dimensions are in millimeters.
2. Solder ball composition: SACQ with CuOSP pads (Sn-4Ag-0.5Cu-3Bi-0.05Ni)

441-Ball Package (Package Code: EK)

Figure 13: 441-Ball TFBGA – 14.0mm (TYP) × 14.0mm (TYP) × 1.1mm (MAX) (Package Code: EK)



Notes: 1. All dimensions are in millimeters.
2. Solder ball composition: SACQ with CuOSP pads (Sn- 4Ag-0.5Cu-3Bi-0.05Ni)

Product-Specific Mode Register Definition

Table 10: Mode Register Contents

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR0	**Per-pin DFE**	**Pre Emphasis**	**Unified NT ODT behavior mode**	**DMI output behavior mode**	**Optimized refresh mode**	**Enhanced WCK always-on mode**	**Latency mode**	**NT ODT timing mode**
	OP[0] = 1b: Device supports different NT ODT latency for DQ and RDQS							
	OP[1] = 0b: Device supports x16 mode latency for 1G16, 1G32, 2G32, 1G64, 2G64 OP[1] = 1b: Device supports x8 mode latency for 4G32							
	OP[2] = 1b: Device supports enhanced WCK always-on mode							
	OP[3] = 1b: Device supports optimized refresh mode							
	OP[4] = 1b: Device supports both DMI behavior mode 1 and 2 and mode selection							
	OP[5] = 1b: The NT ODT behavior follows the unified NT ODT behavior							
	OP[6] = 1b: Device supports Pre Emphasis mode							
	OP[7] = 0b: Device does not support Per Pin DFE							
MR1							**ARFM support[3]**	**CS ODT OP support**
	OP[0] = 1b: Device supports CS ODT behavior OP							
	OP[1] = 1b: Device supports ARFM							
MR3				**BK/BG Org**				
	OP[4:3] = 00b: BG, 01b: 8B, 10b: 16B Mode Supported							
MR5	**Manufacturer ID**							
	1111 1111b: Micron							
MR6	**Revision ID1**							
	0000 0111b							
MR8	**I/O width**		**Density**				**Type**	
	OP[7:6] = 00b: x16 for 1G16, 1G32, 2G32, 1G64, 2G64 OP[7:6] = 01b: x8 for 4G32		OP[5:2] = 0110b: 16Gb				OP[1:0] = 01b: LPDDR5X SDRAM	
MR13						**VRO**		
	OP[2] = 0b: Normal operation (default) 1b: Output the $V_{REF(CA)}$ value on DQ7 and $V_{REF(DQ)}$ value on DQ6							
MR19			**WCK2DQ OSC FM**					
	OP[5] = 1b: WCK2DQ OSC FM supported							

Table 10: Mode Register Contents (Continued)

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR21	**WXS**				**ODTD-CSFS**	**WXFS**	**RDCFS**	**WDCFS**
	OP[0] = 1b: WRITE DATA COPY function supported							
	OP[1] = 1b: READ DATA COPY function supported							
	OP[2] = 1b: WRITE X function supported							
	OP[3] = 1b: Device ODTD-CS is supported							
	OP[7] = 1b: Data to be written can be selected with 0 and 1							
MR22	**RECC**		**WECC**					
	OP[5:4] = 00b: Write link ECC disabled (default) 01b: Write link ECC enabled (See Note 4)							
	OP[7:6] = 00b: Read link ECC disabled (default) 01b: Read link ECC enabled (See Note 4)							
MR24	**DFES**				**Read DCA**			
	OP[3] = 1b: Device supports Read DCA							
	OP[7] = 1b: Device supports DFE (See Note 5)							
MR26		**RDQSTFS**						
	OP[6] = 1b: Read/write-based RDQS_t TRAINING function supported							
MR27	**RAAMULT**		**RAAIMT**					**RFM**
	OP[0] = 1b: RFM is required							
	OP[5:1] = 01110b: 112							
	OP[7:6] = 01b: 4X							
MR41						**DVFSC/ E-DVFSC Support**		
	OP[2:1] = 00b: Only Legacy DVFSC Mode supported							
MR43		**SBEC rule**						
	OP[6] = 1b: Simultaneous SBE on each DQ byte and DMI are independently counted							
MR57	**ARFM[3]**				**RFMSB**		**RAADEC**	
	OP[1:0] = 10b: 2 × RAAIMT							
	OP[3:2] = 00b: 1 = Does not support single-bank mode							
	OP[7:6] = 00b: default (01110b: 112), 01b: Level A = 01101b: 104, Level B = 01100b: 96, Level C = 01011: 88							
MR63 - MR164	Reserved MR bits MR63 through MR164 are RFU by JEDEC standard and should not be accessed by user unless directed by supplier.							

Notes: 1. The contents of mode registers described here reflect information specific to each die in these packages.
2. Refer to General LPDDR5/LPDDR5X Specification 1 for mode registers not described here.
3. Refer to General LPDDR5/LPDDR5X Specification 3 for feature description not described here.
4. Write link ECC and read link ECC are supported.
5. Device supports 3-step DFE.

I_{DD} Parameters

Refer to I_{DD} Specification Parameters and Test Conditions section in General LPDDR5/LPDDR5X Specifications 2 for detailed conditions.

Table 11: WT I_{DD} Parameters – Single Die

Symbol	Supply	Speed Grade				Unit	Note
		x8 Mode		x16 Mode			
		7500 Mb/s	8533 Mb/s	7500 Mb/s	8533 Mb/s		
I_{DD01}	V_{DD1}	3.20	3.20	3.20	3.20	mA	
I_{DD02H}	V_{DD2H}	28.50	28.50	29.00	29.00		
I_{DD02L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD0Q}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD2P1}	V_{DD1}	1.50	1.50	1.50	1.50	mA	
I_{DD2P2H}	V_{DD2H}	2.50	2.50	2.50	2.50		
I_{DD2P2L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD2PQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD2PS1}	V_{DD1}	1.50	1.50	1.50	1.50	mA	
$I_{DD2PS2H}$	V_{DD2H}	2.50	2.50	2.50	2.50		
$I_{DD2PS2L}$	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD2PSQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD2N1}	V_{DD1}	1.50	1.50	1.50	1.50	mA	
I_{DD2N2H}	V_{DD2H}	16.50	16.50	17.00	17.00		
I_{DD2N2L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD2NQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD2NS1}	V_{DD1}	1.50	1.50	1.50	1.50	mA	
$I_{DD2NS2H}$	V_{DD2H}	16.50	16.50	17.00	17.00		
$I_{DD2NS2L}$	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD2NSQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD3P1}	V_{DD1}	1.50	1.50	1.50	1.50	mA	
I_{DD3P2H}	V_{DD2H}	6.50	6.50	6.50	6.50		
I_{DD3P2L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD3PQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD3PS1}	V_{DD1}	1.50	1.50	1.50	1.50	mA	
$I_{DD3PS2H}$	V_{DD2H}	6.50	6.50	6.50	6.50		
$I_{DD3PS2L}$	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD3PSQ}	V_{DDQ}	0.60	0.60	0.60	0.60		

Table 11: WT I_{DD} Parameters – Single Die

Symbol	Supply	Speed Grade				Unit	Note
		x8 Mode		x16 Mode			
		7500 Mb/s	8533 Mb/s	7500 Mb/s	8533 Mb/s		
I_{DD3N1}	V_{DD1}	1.80	1.80	1.80	1.80	mA	
I_{DD3N2H}	V_{DD2H}	20.50	20.50	21.00	21.00		
I_{DD3N2L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD3NQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD3NS1}	V_{DD1}	1.80	1.80	1.80	1.80	mA	
$I_{DD3NS2H}$	V_{DD2H}	20.50	20.50	21.00	21.00		
$I_{DD3NS2L}$	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD3NSQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD4R1}	V_{DD1}	9.00	9.00	11.00	12.00	mA	3, 4
I_{DD4R2H}	V_{DD2H}	295.00	325.00	435.00	485.00		
I_{DD4R2L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD4RQ}	V_{DDQ}	58.00	63.00	116.00	126.00		
I_{DD4W1}	V_{DD1}	8.00	9.00	10.00	11.00	mA	3
I_{DD4W2H}	V_{DD2H}	225.00	245.00	305.00	335.00		
I_{DD4W2L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD4WQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD51}	V_{DD1}	23.00	23.00	23.00	23.00	mA	
I_{DD52H}	V_{DD2H}	165.00	165.00	165.00	165.00		
I_{DD52L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD5Q}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD5AB1}	V_{DD1}	3.20	3.20	3.20	3.20	mA	
$I_{DD5AB2H}$	V_{DD2H}	26.50	26.50	27.00	27.00		
$I_{DD5AB2L}$	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD5ABQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD5PB1}	V_{DD1}	3.20	3.20	3.20	3.20	mA	
$I_{DD5PB2H}$	V_{DD2H}	26.50	26.50	27.00	27.00		
$I_{DD5PB2L}$	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD5PBQ}	V_{DDQ}	0.60	0.60	0.60	0.60		

Notes: 1. Applies to entire table: Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. Applies to entire table: BG mode. DVFSC and DVFSQ disabled.
3. BL = 16, DBI disabled.
4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF; R_{ON} = 40 ohms; T_C = 25°C
5. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V; T_C = –25°C to +85°C

Table 12: WT Full-Array Power-Down Self Refresh Current – Single Die

Temperature	Symbol	Supply	Value	Unit
25°C	I_{DD61}	V_{DD1}	0.27	mA
	I_{DD62H}	V_{DD2H}	0.60	
	I_{DD62L}	V_{DD2L}	(See note 4)	
	I_{DD6Q}	V_{DDQ}	(See note 4)	
85°C	I_{DD61}	V_{DD1}	3.30	
	I_{DD62H}	V_{DD2H}	13.00	
	I_{DD62L}	V_{DD2L}	0.20	
	I_{DD6Q}	V_{DDQ}	0.60	

Notes: 1. I_{DD6}25°C is the typical value in the distribution with nominal V_{DD} and a reference-only value. I_{DD6}85°C is the maximum I_{DD} guaranteed value considering the worst-case conditions of process, temperature, and voltage.
2. DVFSC and DVFSQ disabled.
3. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V; T_C = –25°C to +85°C
4. V_{DD2L} and V_{DDQ} power rails are not used during power-down self refresh.

Table 13: IT I_{DD} Parameters – Single Die

Symbol	Supply	Speed Grade				Unit	Note
		x8 Mode		x16 Mode			
		7500 Mb/s	8533 Mb/s	7500 Mb/s	8533 Mb/s		
I_{DD01}	V_{DD1}	3.30	3.30	3.30	3.30	mA	
I_{DD02H}	V_{DD2H}	30.50	30.50	31.00	31.00		
I_{DD02L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD0Q}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD2P1}	V_{DD1}	1.60	1.60	1.60	1.60	mA	
I_{DD2P2H}	V_{DD2H}	2.70	2.70	2.70	2.70		
I_{DD2P2L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD2PQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD2PS1}	V_{DD1}	1.60	1.60	1.60	1.60	mA	
$I_{DD2PS2H}$	V_{DD2H}	2.70	2.70	2.70	2.70		
$I_{DD2PS2L}$	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD2PSQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD2N1}	V_{DD1}	1.60	1.60	1.60	1.60	mA	
I_{DD2N2H}	V_{DD2H}	17.50	17.50	18.00	18.00		
I_{DD2N2L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD2NQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD2NS1}	V_{DD1}	1.60	1.60	1.60	1.60	mA	
$I_{DD2NS2H}$	V_{DD2H}	17.50	17.50	18.00	18.00		
$I_{DD2NS2L}$	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD2NSQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD3P1}	V_{DD1}	1.60	1.60	1.60	1.60	mA	
I_{DD3P2H}	V_{DD2H}	7.00	7.00	7.00	7.00		
I_{DD3P2L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD3PQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD3PS1}	V_{DD1}	1.60	1.60	1.60	1.60	mA	
$I_{DD3PS2H}$	V_{DD2H}	7.00	7.00	7.00	7.00		
$I_{DD3PS2L}$	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD3PSQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD3N1}	V_{DD1}	1.90	1.90	1.90	1.90	mA	
I_{DD3N2H}	V_{DD2H}	22.50	22.50	23.00	23.00		
I_{DD3N2L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD3NQ}	V_{DDQ}	0.60	0.60	0.60	0.60		

Table 13: IT I_{DD} Parameters – Single Die

Symbol	Supply	Speed Grade				Unit	Note
		x8 Mode		x16 Mode			
		7500 Mb/s	8533 Mb/s	7500 Mb/s	8533 Mb/s		
I_{DD3NS1}	V_{DD1}	1.90	1.90	1.90	1.90	mA	
$I_{DD3NS2H}$	V_{DD2H}	22.50	22.50	23.00	23.00		
$I_{DD3NS2L}$	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD3NSQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD4R1}	V_{DD1}	9.00	10.00	11.00	12.00	mA	3, 4
I_{DD4R2H}	V_{DD2H}	300.00	330.00	440.00	490.00		
I_{DD4R2L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD4RQ}	V_{DDQ}	58.00	63.00	116.00	126.00		
I_{DD4W1}	V_{DD1}	8.00	9.00	10.00	11.00	mA	3
I_{DD4W2H}	V_{DD2H}	230.00	250.00	310.00	340.00		
I_{DD4W2L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD4WQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD51}	V_{DD1}	23.00	23.00	23.00	23.00	mA	
I_{DD52H}	V_{DD2H}	165.00	165.00	165.00	165.00		
I_{DD52L}	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD5Q}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD5AB1}	V_{DD1}	3.20	3.20	3.20	3.20	mA	
$I_{DD5AB2H}$	V_{DD2H}	26.50	26.50	27.00	27.00		
$I_{DD5AB2L}$	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD5ABQ}	V_{DDQ}	0.60	0.60	0.60	0.60		
I_{DD5PB1}	V_{DD1}	3.20	3.20	3.20	3.20	mA	
$I_{DD5PB2H}$	V_{DD2H}	26.50	26.50	27.00	27.00		
$I_{DD5PB2L}$	V_{DD2L}	0.20	0.20	0.20	0.20		
I_{DD5PBQ}	V_{DDQ}	0.60	0.60	0.60	0.60		

Notes: 1. Applies to entire table: Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. Applies to entire table: BG mode. DVFSC and DVFSQ disabled.
3. BL = 16, DBI disabled.
4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF; R_{ON} = 40 ohms; T_C = 25°C
5. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V; T_C = –40°C to +95°C

Table 14: IT Full-Array Power-Down Self Refresh Current – Single Die

Temperature	Symbol	Supply	Value	Unit
25°C	I_{DD61}	V_{DD1}	0.27	mA
	I_{DD62H}	V_{DD2H}	0.60	
	I_{DD62L}	V_{DD2L}	(See note 4)	
	I_{DD6Q}	V_{DDQ}	(See note 4)	
95°C	I_{DD61}	V_{DD1}	3.70	
	I_{DD62H}	V_{DD2H}	16.00	
	I_{DD62L}	V_{DD2L}	0.20	
	I_{DD6Q}	V_{DDQ}	0.60	

Notes: 1. I_{DD6}25°C is the typical value in the distribution with nominal V_{DD} and a reference-only value. I_{DD6}85°C is the maximum I_{DD} guaranteed value considering the worst-case conditions of process, temperature, and voltage.
2. DVFSC and DVFSQ disabled.
3. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V; T_C = –40°C to +95°C